REMARKS

Dear Sir:

These remarks are in response to the Office Action mailed on January 9, 2004, for which a two-month extension is requested. The Office Action rejected claims 1-38 under 35 U.S.C. 102(b) as anticipated by Estakhri et al. (U.S. patent number 5,907,856). For the reasons given below, it is respectfully submitted that the pending claims are allowable.

Claims 1-10

The Office Action is correct in that Estakhri describes techniques for using mapping information that associates logical addresses with physical addresses for "original" locations and "moved" locations; however, the teachings of Estakhri differ from the aspects of the present invention found in the pending claims in a number of ways. More specifically, with respect to claim 1, in the cited location, Estakhri (beginning at column 11, line 64) describes a "table 700 store[s] information generally representing a PBA [physical block address] value corresponding to a particular LBA [logical block address] value." As is clear in the discussion leading to the location cited in the Office Action, Estakhri places this table in the RAM memory of the controller: "table 700 in SPM RAM blocks 548 configured to store LBA-PBA mapping information" (column 11, lines 18-19). As is clear form Figure 10 of Estakhri, the SPM RAM 548 is contained in the space management block 544 that is *part of the controller 506.*

In contrast, claim 1 of the present invention presents:

> A non-volatile memory system comprising:
> a controller ... and
> a memory connected to the controller, comprising...
> an array ... and
> a pointer structure storing correspondences between logical sector addresses and physical sector addresses ...

According to the invention of claim 1, the pointer structure is part *of the memory, not* the controller. Aside from the differences (discussed in the following) between the pointer structure of claim 1 itself and the table of Estakhri, which the Office Action is identifying with this pointer structure, the invention of claim 1 differs from the prior art in that it places a pointer structure on the memory itself.

In Figure 10, Estakhri shows a memory system 500 that consists of a controller 506 and memory unit 508 having flash memory units 510-512. As is standard in the prior art, the logical to physical address conversion, which in Estakhri is based on multi-sector blocks, is performed on the controller, with communication between the controller 506 and memory unit 508 using the physical addresses. In Estakhri, the conversion is performed using SPM RAM 548. This distinction from the present invention can be illustrated by comparing Estakhri's Figure 10 with Figure 1 of the present application, where the pointer structure 110 forms part of the memory 103, not part of controller 101.

Estakhri neither teaches nor suggests "a pointer structure" located *on the memory*, instead of the controller; additionally, Estakhri neither teaches nor suggests a pointer structure on the memory that "concurrently maintains a *first correspondence* between a logical sector address and a first physical sector address at which currently valid data identified by the logical sector address is stored and a *second correspondence* between the logical sector address and a second distinct physical sector address at which previously valid data identified by the logical sector address has been stored."(emphasis added) The table used by Estakhri employs a differ structure than the "pointer structure" as presented in claim 1.

More specifically, both in the cited portions (column 11, line 64, to column 12, line 20) and elsewhere, Estakhri describes a table structure where a logical block address (LBA value) corresponds to a single physical block address (PBA value). As sectors within logical block are updated, the new version of the sectors written into other blocks, where these blocks are then linked (using "MVPBA block addresses" and various flags) to the physical block address. Thus, Estakhri describes a structure where that maintain *only a single correspondence between a given logical block address and a first physical block*, with possibly newer versions of sectors within the logical block linked to this first physical block through this chain-like linking structure. Estakhri neither describes nor suggests concurrently maintaining a second correspondence between the given logical block address and a second physical block, where one of these correspondences contains currently valid data and the other contains previously valid data. Consequently, the teachings of Estakhri are distinct from the final limitation of the present invention, namely,

> wherein the pointer structure *concurrently* maintains *a first correspondence between a logical sector address and a first physical sector address* at which currently valid data identified by the logical sector address is stored and *a second correspondence between the logical sector address and a second distinct physical sector address* at which previously valid data identified by the logical sector address has been stored. (emphasis added)

This is illustrated in Figure 2 of the present application, where both the "new PSA" and "old PSA" are shown as corresponding the "LSA" in the pointer structure 110.

Consequently, for any of these reasons, it is respectfully submitted that a rejection of claim 1 and dependent claims 2-10 under 35 U.S.C. 102(b) as anticipated by Estakhri is not well founded and should be withdrawn.

Concerning claim 2, the Office Action refers to column 6, lines 22-25, of Estakhri. This portion refers to the keeping of a "shadow" copy of the mapping information in non-volatile memory. This is not part of what the Office Action is identifying as the "pointer structure"; rather, it is a backup copy of some of the mapping information that is kept in the non-volatile memory and occasionally updated so that, if power is lost, this information can be retrieved by the mapping table. Additionally, this "shadow copy" only holds current copies of such logical to physical mappings ("logical block address with the *active* physical block address ... is also stored as a shadow memory", col. 6, lns. 23-25, emphasis added) and, consequently, does not meet the limitations required of the "pointer structure" of holding both *currently* and *previously* valid correspondences. Consequently, claim 2 and dependent claims 3 and 4 are further believed allowable for these reasons.

With respect to claim 3, claim 3 depends upon claim 2. The Office Action cites column 10, lines 15-17, of Estakhri. This portion refers to the structure of the space manager block 544 formed in volatile RAM on the controller. Although Estakhri does not explicitly say so, the Office Action is correct in that it would presumably have a separate decoder structure from the memory array. However, according to claim 3, the pointer structure is required to be on the memory and storing the correspondences in non-volatile elements there which have a distinct decoder from the array. It is respectfully submitted that Estakhri has no teaching or suggestion of this. Further, for the "shadow copy", which the Office Action has referred to in claim 2, this is stored in the regular flash array and, as such, would instead share the same decoder structure as the rest of the array. Claim 3 is believed further allowable for any of these reasons.

With respect to claim 4, claim 4 also depends upon claim 2. The Office Action cites column 12, line 50. to column 13, line 5, of Estakhri. This portion again refers to the structure of the space manager block 544 formed in volatile RAM on the controller, not to non-volatile

storage elements on the memory. According to claim 4, the pointer structure is required to be on the memory and storing the correspondences in non-volatile elements there which are binary, while using multi-state elements for data storage. Claim 4 is believed further allowable for these reasons.

Concerning claim 6, it is respectfully submitted that Estakhri does not maintain both "currently valid data identified by the logical sector address *and* previously valid data identified by the logical sector address", where the emphasis is added. Rather, Estakhri uses the sort of chain-like structure described above, where a logical block address is linked to a single physical block address. This first physical block address may then be linked to a second physical block to indicate where newer versions of sectors within the block can be found, but the logical block address identifies only a single physical block. Claim 6 is believed further allowable for these reasons.

With respect to claim 7, the Office Action cites column 9, lines 34-50, and column 11, line 64, to column 12, line 20, of Estakhri. This first of these sections is a discussion error correction code (ECC) to correct corrupted data. The sector describes the linking mechanism whereby, starting with the logical block to physical block conversion information, updated versions of sectors within the block can be found. In neither location is there a discussion of how, "in response to a command", the controller can *access previously valid data* identified with a logical address. Claim 7 is believed further allowable for these reasons.

With respect to claim 8, the Office Action also cites column 11, line 64, to column 12, line 20, of Estakhri. This section again refers to mapping information in a table in the volatile RAM of the controller, rather that on the memory. Consequently, there is not discussion of "write circuitry coupled to the memory array and the pointer structure". Additionally, no discussion of writing new data into the array and concurrently writing the corresponding new correspondence into what the Office Action identifies as the pointer structure can be found. Claim 8 is believed further allowable for any of these reasons.

Claims 11-19

Claim 11 is drawn to an integrated circuit having a non-volatile memory array that transfers data externally to the circuit based on logical sector addresses. As with the memory of claim 1, the integrated circuit of claim 11 contains a pointer structure for storing correspondences between logical and physical sector addresses,

> wherein the pointer structure *concurrently* maintains a *first correspondence between a first logical sector address and a first physical sector address* at which currently valid data identified by the first logical sector address is stored and *a second correspondence between the first logical sector address and a second distinct physical sector address* at which previously valid data identified by the first logical sector address has been stored.

As again indicated by the added emphasis, the pointer structure of claim 11 can concurrently maintain logical to physical sector correspondences for both currently valid data *and* previously valid data. As discussed above with respect to claim 1, this is distinct from the teachings of Estakhri, where only a single correspondence between a given logical block address and a physical block address is maintained, a chain-like linking between different physical blocks then being employed for sectors within the logical block that have been updated.

Consequently, for any of these reasons, it is respectfully submitted that a rejection of claim 10 and dependent claims 11-19 under 35 U.S.C. 102(b) as anticipated by Estakhri is not well founded and should be withdrawn. Additionally, many of dependent claims 12-19 are believed to be further allowable for the reasons given above with respect to the corresponding ones of dependent claims 2-10 (where the correspondence is as is noted in the Office Action).

Claims 20-28

Method claim 20 is similar to the device claim of claim 1. It again relates to "a memory system comprising a controller and a memory, the *memory including a pointer structure* ...", where, as the added emphasis indicates, the pointer is again part of the memory, in contrast to Estakhri, which uses a table on the controller.

Claim 20 also contains the step of "*transferring* the first data set and *the logical sector address from the controller to the memory*". As the added emphasis indicates, the controller communicates with the memory using the *logical* address, where the correspondence between the logical address and the physical address is maintained in the pointer (110, Figures 1 and 2) on the memory itself. This is in contrast to prior art in general, and the teachings of Estakhri

in particular, where the logical to physical conversion is performed by the controller, which then communicates with the memory based upon physical addresses. This can again been seen by comparing Figure 10 of Estakhri, where the logical address received from the host 502 along line 504 are converted using tables in SPM RAM 548 on controller 506 to the physical address that will be used by the controller to communicate with the memory 508, with Figure 1 of the present application, where the logical address (LSA) is received from the host at the controller 101 and passed on to pointer structure 110 on the controller 103 where it is there associated with a physical address (PSA).

Claim 20 further stores "a second correspondence between the logical sector address and the second physical sector address in the pointer structure, wherein the memory retains ... the first correspondence in the pointer structure subsequent to said storing the second data set and said storing the second correspondence." As discussed above with respect to claims 1 and 11, Estakhri only maintains a single correspondence between a given logical address and any physical address, relying upon a chain structure of physical addresses for any updates prior to establishing a new, single such correspondence.

Consequently, for any of these reasons, it is respectfully submitted that a rejection of claim 10 and dependent claims 20-28 under 35 U.S.C. 102(b) as anticipated by Estakhri is not well founded and should be withdrawn.

Dependent claims 21, 24, and 26 are believed to be further allowable for the same reasons given above with respect to claims 8, 2 and 7, respectively. Claim 25 is believed further allowable as it describes a read process where the controller accesses data from the memory based on a *logical* address, instead of using a physical address as is found in the prior art.

Claims 29-37

Method claim 29 is similar to the device claim of claim 11 and believed allowable for much the same reasons as described above for claim 11. More explicitly, its final element is

> storing a second correspondence between the logical sector address and the second physical sector in the pointer structure, wherein the first data set is retained in the first physical sector address and *the first correspondence is retained in the pointer subsequent to writing the second data set and storing the second correspondence.*

As the added emphasis indicates and is discussed with respect to the above independent claims, this is again contrary to the teachings of Estakhri, where only a single correspondence is maintained in its table structure for a given logical address. Consequently, it is respectfully submitted that a rejection of claim 29 and dependent claims 30-37 under 35 U.S.C. 102(b) as anticipated by Estakhri is not well founded and should be withdrawn.

Dependent claims 30, 33, and 35 are believed to be further allowable for the same reasons given above with respect to claims 8, 2 and 7, respectively.

Claim 38

With respect to claim 38, it is respectfully submitted that the rejection 35 U.S.C. 102(b) as anticipated by Estakhri is not well founded. Claim 38 states:

> A method of operating a non-volatile memory system comprising a controller and a memory, wherein data is stored in the memory based on physical address, the method comprising:
>
> transferring data between a host and the controller based on a logical sector addresses;
>
> *transferring data between the controller and the memory based on the logical sector address;*
>
> *converting on the memory the logical sector address into a corresponding physical sector address*; and
>
> accessing data stored in the memory at the corresponding physical address.

Among other reasons, this is believed to differ from Estakhri, and the prior art in general, based upon the middle two elements, which have the added emphasis. As described in the claim, data is exchanged between the controller and memory based on the *logical address*, which is then converted *on the memory* itself into a physical address. This is the reverse of what occurs in the cited prior art, where the logical to physical address conversion takes place *on the controller*, with data then being transferred between the controller and the memory based on the already converter *physical address*. In both cases, the first and last elements of the claim would be the same, but it is the middle two elements that distinguish it from the prior art, resulting in the advantages cited in the application.

This can again been seen by comparing Figure 10 of Estakhri, where the logical address is received from the host 502 along line 504 are converted using tables in SPM RAM 548 on controller 506 to the physical address that will be used by the controller to communicate with the memory 508, with Figure 1 of the present application, where the logical address (LSA) is received from the host at the controller 101 and passed on to pointer

structure 110 on the controller 103 where it is there associated with a physical address (PSA). Consequently, there is no "converting on the memory the logical sector address into a corresponding physical sector address" in Estakhri.

Consequently, it is respectfully submitted that a rejection of claim 38 under 35 U.S.C. 102(b) as anticipated by Estakhri is not well founded and that, for these reasons, claim 38 is also believed allowable.

Conclusion

For any of the above reasons it is respectfully submitted that a rejection of claims 1-38 under 35 U.S.C. 102(b) as anticipated by Estakhri is not well founded is not well founded and should be withdrawn. Reconsideration of claims 1-38 and an early indication of their allowance are respectfully requested.

Respectfully submitted,

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